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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,682	12/07/2005	Martin Wany	Q96159	6166

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EXAMINER	
WILLIAMS, DON J	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,682	WANY ET AL.	
	Examiner	Art Unit	
	Don Williams	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5, 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection. New claims 17-20 have been added. Claim 6 has been cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9, 15, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozlowski et al (6,587,142).

As to claim 1, Kozlowski et al disclose (fig. 3) one photodiode (12) having a photodiode capacitance (C_{PD}), a first transistor (M_3) connected between photodiode (12) and a first potential (ΦRST), first transistor (M_3) having a channel and a gate connected to a first gate voltage (3.3V), a readout amplifier (50) having an input and an output, a storage means (C_{STORE}, C_{FB}, C_{PD}) connected to the input of readout amplifier (50) to allow temporary storage of a signal value (photo-induced charge) at the input of the readout amplifier (50) during a holding time (microseconds) and until a readout time (microseconds), a second transistor (M_1) connected between photodiode (12) and the input of readout amplifier (50) in order to provide a large dynamic range, second transistor (M_1) having a gate connected to a second gate voltage (2.5V), and a third

transistor (M_2) connected between the input of the readout amplifier (50) and a second potential (V_{RST}, V_{DD}), the optoelectronic sensor (10) being operable to change signal value (2.5V, 3.3V) at the input of the readout amplifier (50) due to light impinging on photodiode (12) during an integration time (microseconds), the integration time (microseconds) reading out one row at a time constituting a first phase and a last phase, wherein second gate voltage (2.5V) is controllable so that a current (photo-induced charge) generated by the photodiode (12) discharges only storage means (C_{STORE}, C_{FB}, C_{PD}) in the first phase of the integration time (microseconds), and wherein the first gate voltage (3.3V) if there is a first transistor (M3) is controllable so that some or all of the current (photo-induced charge) generated by the photodiode (12) is compensated (gain) for by the channel of the first transistor (M1) respectively in the last phase of the integration time (microseconds), (column 7, lines 63-67, column 8, lines 1-55).

As to claim 2, Kozlowski et al disclose (fig. 2) first potential (Vrst) and second potential (Vdd) share a voltage that is set at (2.5V) which constitutes identical voltage level, (column 7, lines 25-26).

As to claim 3, Kozlowski et al disclose (fig. 2) storage means comprise a conversion node capacitance (C_{STORE}, C_{FB}) connected between the input of the readout amplifier (50) and a ground potential.

As to claim 4, Kozlowski et al disclose (fig. 3) a row selection transistor (M2) and a column bus (20), the output of the readout amplifier (50) being connected to the

column bus (20) via the row selection transistor (M2), (column 8, lines 9-10, lines 36-38).

As to claim 5, Kozlowski et al disclose transistors (M1-M4) are MOS transistors, (column 7, lines 38-44).

As to claim 9, Kozlowski et al disclose the first gate voltage (3.3V) of the first transistor (M3) and the second gate voltage (2.5V) of the second transistor (M1) are variable during integration time (fig. 3, column 7, lines 63-67, column 8, lines 1-10, lines 24-28).

As to claim 15, Kozlowski et al disclose a one-or two dimensional imaging array of optoelectronic sensors (10), (fig. 2, column 4, lines 40-41).

As to claim 18, Kozlowski et al disclose second transistor (M1) is operable to be open at the end of integration time so that a signal is held in the storage means (C_{STORE}, C_{FB}, C_{PD}) during a holding time (microseconds) and until readout time (microseconds), wherein the first transistor (M3) is operable to be adjusted during this holding time (microseconds) so that the photodiode capacitance (C_{PD}) is not fully discharge, (column 7, lines 62-67, column 9, lines 1-5, lines 25-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-8, 10-14, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski et al (6,587,142).

As to claim 7, Kozlowski et al disclose a first transistor (M3), a first gate voltage (3.3V), a second gate voltage (2.5V), and a readout amplifier (50), (column 8, lines 5-6, lines 27-31, lines 35-37). Kozlowski et al also disclose a threshold voltage (REF1), (column 9, lines 52-53). Kozlowski et al is silent of explicitly disclosing the first gate voltage is lower than the second gate voltage and the first gate voltage is higher than a saturation signal of the readout amplifier by a threshold voltage. Kozlowski et al does disclose a threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), (fig. 4, column 9, lines 46-49). It would have been obvious for one of ordinary skill in the art to integrally use the first transistor, first gate voltage, second gate voltage, readout amplifier, and reference voltage as disclosed by Kozlowski et al in order to determine the varied values of the gate voltages and saturation signals to ensure charge carriers accumulated by the photodiode discharge at a suitable integration time corresponding to the intensity distribution of the incident light over an array of sensor cells.

As to claim 8, Kozlowski et al disclose (fig. 3) first transistor (M1), second transistor (M2), first gate voltage (3.3V), and second gate voltage (2.5V), (column 8, lines 1-10, lines 24-29). Kozlowski et al also disclose threshold voltage (REF1), (column 9, lines 51-53). Kozlowski et al is silent of explicitly disclosing a difference being greater than the tolerances of the threshold voltage plus the tolerances of the first

and second gate voltages. It would have been obvious for one of ordinary skill in the art to integrally use the first transistor, first gate voltage, second gate voltage, readout amplifier, and reference voltage as disclosed by Kozlowski et al to determine the tolerances of the threshold voltages and the tolerances of the gate voltages to ensure charge carriers accumulated by the photodiode discharge at a suitable integration time.

As to claim 10, Kozlowski et al disclose photodiode (12) having a photodiode capacitance (C_{PD}), a first transistor (M3) connected between photodiode (12) and a first potential (ΦRST), first transistor (M3) having a channel and a gate connected to a first voltage (3.5V), a readout amplifier (50) having an input and an output, a conversion node capacitance (C_{STORE}, C_{FB}) connected to the input of readout amplifier (50) to allow temporary storage of a signal value (photo-induced charge) at the input of the readout amplifier (50) during a holding time (microseconds), a second transistor (M1) connected between photodiode (12) and the input of readout amplifier (50), second transistor (M1) having a gate connected to a second gate voltage (2.5V), and a third transistor (M2) connected between the input of the readout amplifier (50) and a second potential (V_{RST}, V_{DD}), the method comprising controlling the first gate voltage (3.5V) if there is a first transistor (M3) and controlling the second gate voltage (2.5V) of the second transistor (M1) during an integration time, the integration time preceding the holding time (microseconds) and wherein the photodetectors (12) readout a prescribed integration time one row at a time constituting having a first, a second, and a third phase so that charge carriers (photo-induced charge) accumulated by the photodiode (12) discharge only conversion node capacitance (C_{STORE}, C_{FB}) in the first phase of the integration time

that charge carriers (photo-induced charge) accumulated by the photodiode (12) discharge both the photodiode (12) and conversion node capacitance (C_{STORE}, C_{FB}) in the second phase of the integration time, (column 7, lines 25-26) the second phase beginning after an equal potential (shared potential, 2.5V) has been reached at the output of the photodiode (12) and the input of the readout amplifier (50), charge carriers (photo-induced charge) accumulated by the photodiode (12) are made available via the first transistor (M1) in the third phase of the integration time, (column 7, lines 63-67, column 8, lines 1-55). Kozlowski et al fail to explicitly disclose after the output of the photodiode has fallen below the threshold value of the first transistor. Kozlowski et al does disclose (fig. 4) a threshold value (REF1) and that a threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), (column 9, lines 47-53). It would have been obvious for one of ordinary skill in the art to include an amplifier to allow threshold adjustment in order to ensure that the charge carriers outputted by the photodiode are below the threshold value resulting in a suitable integration time corresponding to the light intensity over an array of sensor cells.

As to claim 11, Kozlowski et al disclose a second gate voltage (2.5V), a second transistor (M1), and integration time, (column 8, lines 5-8). Kozlowski et al is silent of disclosing the second gate voltage minus a threshold voltage of the second transistor is lower than a reset voltage which is set at the input of the readout amplifier and wherein the second gate voltage is higher than a saturation voltage of the readout buffer by a threshold voltage. Kozlowski et al does disclose a threshold voltage (reference voltage,

REF1), and that a threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), column 9, lines 47-52). It would have been obvious for one of ordinary skill in the art to include an amplifier capable of threshold adjustments to set the second gate voltage minus a threshold voltage of the second transistor lower than a reset voltage and to set a second gate voltage higher than a saturation voltage of the readout buffer in order to ensure that the charge carriers outputted by the photodiode result in a suitable integration time corresponding to the light intensity over an array of sensor cells.

As to claim 12, Kozlowski et al disclose first gate voltage (3.5V), second gate voltage (2.5V), integration time, (column 7, lines 63-67, column 8, lines 5-10, lines 24-31). Kozlowski et al is silent of disclosing second gate voltage is varied during the integration time although it remains greater than the first gate voltage. Kozlowski et al does disclose a threshold voltage (reference voltage, REF1), and that a threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), column 9, lines 47-52). It would have been obvious for one of ordinary skill in the art to use the amplifier to adjust the threshold voltage as disclosed by Kozlowski et al in order to determine the varied values of the gate voltages and to ensure that the second gate voltage remains greater than the first gate voltage to ensure charge carriers accumulated by the photodiode discharge at a suitable integration time corresponding to the intensity distribution of the incident light over an array of sensor cells.

As to claim 13, Kozlowski et al disclose the first gate voltage (3.3V) and integration time, (column 7, lines 63-67, column 8, lines 25-30). Kozlowski et al is silent of disclosing first gate voltage is kept constant or successively reduced during integration time. Kozlowski et al does disclose a threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), column 9, lines 47-52). It would have been obvious for one of ordinary skill in the art to use the amplifier as disclosed by Kozlowski et al to ensure that the first gate voltage is kept constant or successively reduced during integration time resulting in charge carriers accumulated by the photodiode discharge at a suitable integration time corresponding to the intensity distribution of the incident light over an array of sensors.

As to claim 14, Kozlowski et al disclose second gate voltage (3.3V), a bulk potential (V_{RST}, V_{DD}) of the second transistor (M1), (column 8, lines 5-15, lines 25-30). Kozlowski et al is silent of the second transistor is switched back again to its original value. Kozlowski et al does disclose second transistor (M1) discharge from the reset voltage (Vrst) to a lower voltage, the discharge rate depends directly upon the incident signal, the photodetectors (12) are readout from left to right, and in preparation for reading and resetting each row, (V_{rst}) is set to about 2.5V, (column 8, lines 1-7). It would have been obvious for one of ordinary skill in the art to use the second transistor as disclosed by Kozlowski et al to switch or reset at least once so that it is equal to a bulk potential of the second transistor and is switch or reset back again to its original value resulting in charge carriers accumulated by the photodiode discharge at a suitable

integration time corresponding to the intensity distribution of the incident light over an array of sensors.

As to clam 16, Kozlowski et al disclose all the active pixels in a row in a one-or two-dimensional imaging array are reset on a row-by-row basis constitutes operating an array (column 4, lines 39-41).

As to claim 17, Kozlowski et al disclose an integration time, an equal potential (2.5V) has been reached at the output of the photodiode (12) and at the input of the readout amplifier (50), and wherein the optoelectronic sensor (10) is operable so that charge carriers (photo-induced charge) accumulated by the photodiode (12) discharge both the photodiode capacitance (C_{PD}) and conversion node capacitance (C_{STORE}, C_{FB}), (column 7, lines 25-27, column 8, lines 1-5, lines 30-51). Kozlowski et al is silent of explicitly disclosing the integration time has a second phase between the first phase and the last phase and the output of the photodiode has fallen below the threshold value of the first transistor. Kozlowski et al does disclose the signals from the photodetectors (12) are readout after a prescribed integration time one row at a time, from bottom to top of the array, (column 7, lines 63-65). Kozlowski et al also disclose threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), (column 9, lines 47-49). It would have been obvious for one of ordinary skill in the art to include an amplifier that is capable of reading out the signals one row at a time corresponding to phases of the readout signals resulting in photo-induced charge or output falling below the threshold value of the transistor in order to ensure charge carriers accumulated by the photodiode discharge at a suitable

integration time corresponding to the intensity distribution of the incident light over an array of sensor cells.

As to claim 19, Kozlowski et al disclose the first diode (12) is present, (column 7, lines 62-67). Kozlowski et al does disclose a first potential (V_{RST}), and a second gate voltage, (2.5), (column 8, lines 1-5). Kozlowski et al is silent of explicitly disclosing first diode has a diode threshold voltage and a diode anode voltage, the diode anode voltage being adjustable by the first potential in a manner that the anode voltage minus the diode threshold voltage is lower than the second gate voltage minus a threshold voltage of the second transistor, and wherein the diode anode voltage is higher than a saturation signal of the readout amplifier by the diode threshold voltage. Kozlowski et al does disclose a reference voltage (REF1) and that a threshold adjustment is obtained by placing a low transconductance amplifier (72) in parallel with the main amplifier (62), column 9, lines 47-50). It would have been obvious for one of ordinary skill in the art to include an amplifier capable of threshold adjustments in order to set the anode voltage minus the diode threshold voltage lower than the second gate voltage minus a threshold voltage of the second transistor and to set a second diode voltage higher than a saturation signal of the readout amplifier in order to ensure that the charge carriers outputted by the photodiode result in a suitable integration time corresponding to the light intensity over an array of sensor cells.

As to claim 20, Kozlowski et al disclose opening second transistor (M1) after the integration time has elapsed so that the signal (photo-induce charge) is held at the conversion node capacitance (C_{STORE}, C_{FB}), during the holding time (microseconds) and

until a readout time (microseconds), wherein the first transistor (M3) is adjusted during this holding time (microseconds) so that the photodiode capacitance (C_{PD}), is not fully discharged, (column 7, lines 63-67, column 8, lines 1-5, lines 25-55).

Conclusion

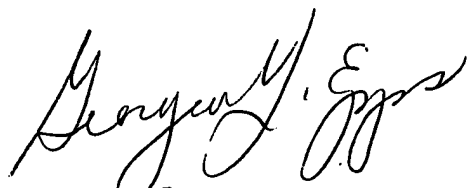
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don Williams whose telephone number is 571-272-8538. The examiner can normally be reached on 8:30a.m. to 5:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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